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HIGH-EFFICIENCY FIVE-LEVEL BOOST MULTILEVEL INVERTER FOR GRID-TIED SOLAR SYSTEMS

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ABSTRACT: The voltage is insufficient. Power electronic converters are employed in energy-changing systems to generate energy that is sustainable. This research addresses an innovative REGS application that utilizes a single capacitor boost in a multilayer inverter that is connected to a single-phase grid. Multilevel inverters are advantageous for medium- to high-power applications. This article introduces a novel boost multilevel inverter that necessitates only one capacitor and has five levels: 2Vdc, Vdc, 0, −Vdc, and −2Vdc. The single-phase configuration is comprised of eight switches, one capacitor, and one DC source. The charge-pump design of the inverter results in a significant increase in power. This theory contends that the output voltage is increased by the charging and discharging of series and parallel capacitors. By comparing the reference signal to four carriers, levelshift pulse width modulation generates the appropriate pulse pattern. This straightforward method regulates the valves in the manner depicted. The inverter is distinctive in that it is compact, user-friendly, and requires only a DC source and capacitor to operate. Additionally, it provides a boost. MATLAB is employed to generate system models. The operation of the new five-level grid-connected solar system is verified by this simulation.

Keywords: five-level, multilevel inverter, Energy Generation Systems (REGS), pulse width modulation.

1.INTRODUCTION

Renewable energy systems must convert from DC to AC in order to generate AC with a specific amplitude, frequency, and low harmonic profile. Pulse width modulation (PWM) is employed by inverters in numerous power electronics systems to transition between DC and AC. These inverters are capable of operating at multiple levels. These devices allow for the modification of output voltage frequency, amplitude, and harmonics. AC output harmonics are diminished by multilayer inverters. Multilayer inverter topologies are preferred by academics due to their enhancement of narrow filters and output waveforms. Using power semiconductors, multilevel inverters combine DC levels to generate a staircase waveform. Multilevel inverters exhibit superior harmonic characteristics and voltage stresses on semiconductors. Multilayer inverters that operate at a higher level generate an increased amount of electricity. Nevertheless, semiconductor power and circuits expand as levels increase. Consequently, the system is both costly and perplexing. This impacts the utility and reliability of the system. There are numerous methods for organizing multilayer inverters. These systems include modular multilevel converters, modular multilevel converters, CHB, and NPC. These multilevel systems generate voltage levels of three, five, seven, or n. The NPC inverter, a three-level diode-clamped motor controller, was developed by Akagi and Nabae. This design presents numerous challenges in terms of DC capacitor stability and equilibrium due to the presence of only one DC supply. The voltage and current of DC capacitors are regulated by DC supplies. It is impossible for two stacks to collapse and injure themselves. An FC multilevel converter was employed by Stillwell and PilawaPodgurski to restrict the voltage at one capacitor level, rather than a clamping diode. Phase redundancy distinguishes the FC multilevel inverter from the NPC. This FC component is responsible for addressing voltage concerns and assist with charging and discharging.

Voltage stresses and harmonic profiles are enhanced by the implementation of two power relays. FC multilayer inverters encounter challenges. For example, its switching is insufficient, and it is unable to regulate the voltage of all capacitors. The CHB multilevel converter is distinctive in that it employs H-bridge inverters in a series. A DC source is present on each bridge. It is capable of being modified, rendering it superior to neutral point and FC configurations. This enables the inverter to operate at a reduced power level while simultaneously adjusting in the event of a cell failure. A modular multilayer inverter is an additional customizable option. This scenario contains infinite layers due to the stacking of submodules with varying control mechanisms. Balancing the submodule capacitor is the most challenging aspect of modular multilevel topologies. This is due to the fact that the current of the converter decreases the capacity of the system. A five-level boost inverter that is intriguing is the focus of this investigation. Numerous five-level arrangements are described in the literature. A five-level output can be generated by six switches, two diodes, and two capacitors, as illustrated in. The system is less effective due to the fact that it necessitates a complex management algorithm to balance capacitors and diodes, while having fewer switches.

The two conceptions are similar in that they both employ switched capacitor cells and aim for nine layers rather than five. Roy et al. developed the most basic cross-switched inverter by employing switched-capacitor converters. The five-level variant is more difficult to operate due to the presence of two capacitors. The reference illustrates an alternative five-level architecture. The five-level output is generated by seven switches, four diodes, and two capacitors. A variety of inverters are arranged in the new configuration. The following topologies necessitate six DC sources for three-phase or two DC sources with varying voltage amplitudes for nine levels. In contrast, the proposed study has the potential to generate voltage at five levels by utilizing a direct current source, a capacitor, and three phases. This necessitates only one DC source to generate a three-phase output voltage. The proposed design is more effective than the previous one in that it can increase the

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output voltage to over twice the input voltage. A five-level output voltage that is twice as potent as the input voltage is generated by a single direct current source, one capacitor, and eight power switches. The output voltage levels are as follows: two Vdc, Vdc, zero, → Vdc, and −2Vdc. The proposed system is illustrated in its most basic form in the diagram. 1.

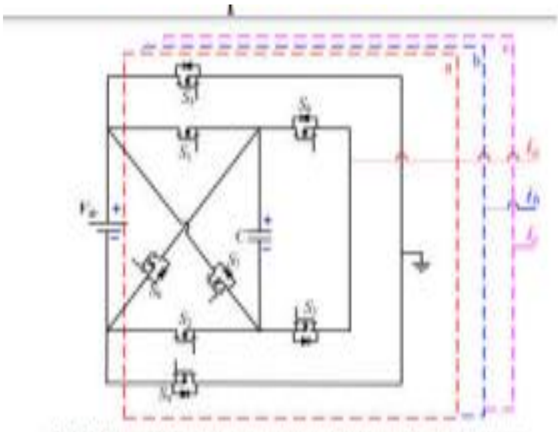


Fig. 1 General Schematic representation of proposed five-level inverter

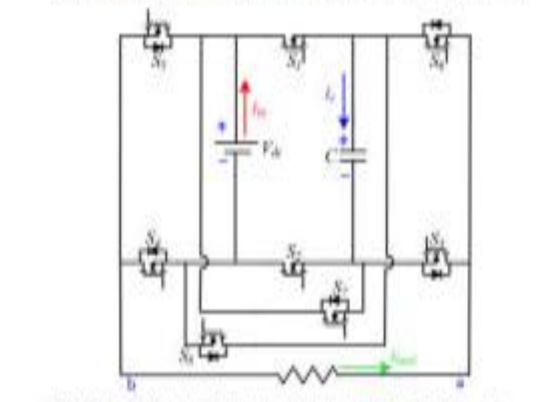
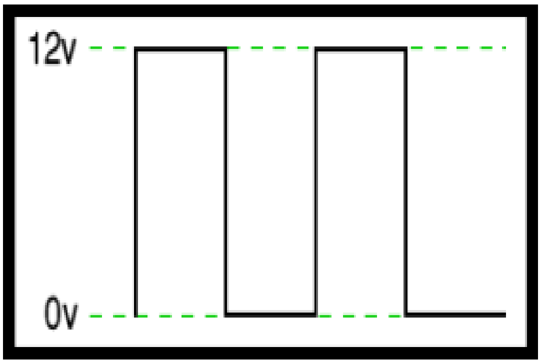


Fig. 2 Single-phase configuration of the proposed five-level inverter

2. PULSE WIDTH MODULATION

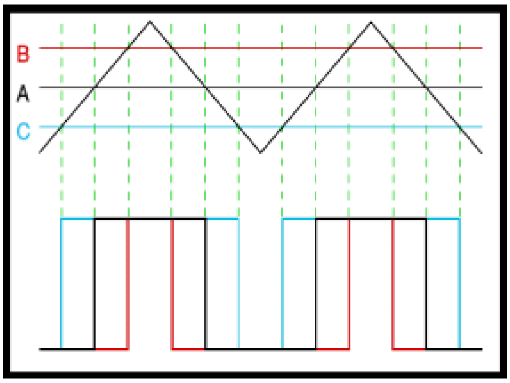
PWM

PWM is the most effective method for consistently charging batteries and activating the power sections of the solar system controller. The PWM regulation current of a PV array is determined by the battery's current level and charging requirements. A "suitable device" connected to the output will produce an average of 6 V, which is half of 12 V. This is due to the fact that 0 V has the same duration as 12 V. The "average" voltage is altered by adjusting the positive pulse breadth.



Pulse Width modulator

The circuits are easily accessible on the TEC website. Draw the triangle waveform provided below. This court is legitimate. Alter the voltage to achieve the appropriate on-to-off ratio. The output increases in proportion as the triangle crosses the "demand" voltage. It ceases to function when the voltage falls below the triangle.



3. MULTI LEVEL INVERTER

Transformers, switches, and control circuits are employed by inverters to convert DC to AC. AC can be produced at any voltage and frequency. The applications of static inverters are diverse, ranging from the transfer of large

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quantities of electricity by electric utilities to the powering of small computers and the operation of massive high-voltage direct current systems. Static inverters are distinctive in that they lack any movable components. When solar panels or batteries are employed, inverters convert DC power into AC power. When fully activated, the electrical inverter functions similarly to an electronic oscillator. The initial mechanical AC-to-DC converters functioned in reverse, or "inverted," to convert DC to AC. The term "inverted" is derived from this.

Cascaded H-Bridges inverter

The image illustrates the single-phase multilayer cascaded inverter construction. Each distinct DC source is connected by an H-bridge, or single-phase complete bridge inverter. Each inverter level can generate one of three voltage outputs by modifying the DC source to the AC output for each of the four switches (S1, S2, S3, and S4). In order to acquire +Vdc, activate S1 and S4. Activate the -Vdc switches S2 and S3. The output voltage is reduced to zero by engaging switches S1 and S2 or S3 and S4. The AC outputs of each bridge inverter level connected in series are averaged to generate the synthetic voltage waveform. The output phase voltage levels of a cascade inverter are determined by the number of DC sources (s) multiplied by two. utilizing the formula m = 2s + 1. The graphic illustrates an 11-level cascaded H-bridge inverter that contains five complete bridges, five SDCSs, and eleven levels.

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$$

The voltage phase is consistent. demonstrates an s-step waveform and a Fourier Transform.

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n[\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\frac{\sin(n\omega t)}{n}, \text{ where } n = 1,3,5,7\ldots$$

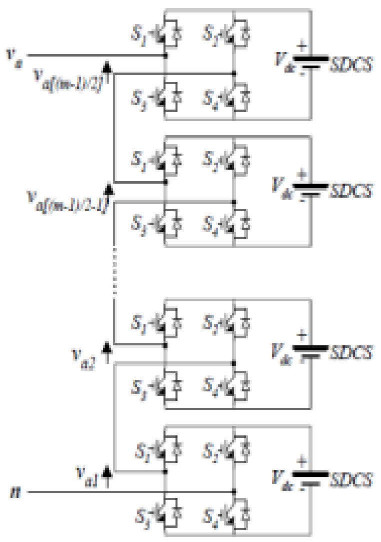

Fig.Single-phase structure of a multilevel cascaded H-bridges inverter

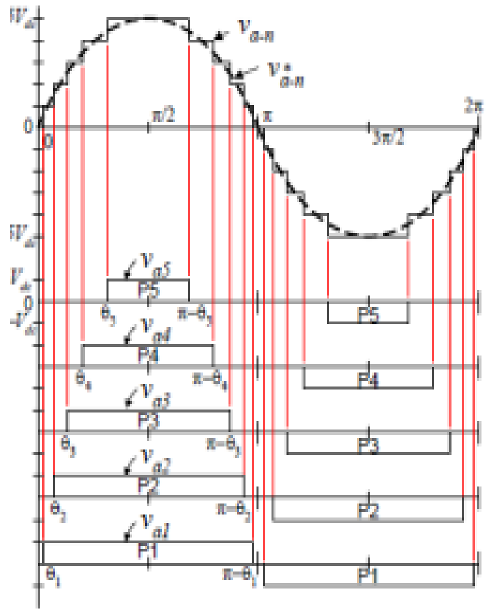

Fig. Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources

4.PROPOSED SYTEM AND CONTROL DESIGN

Proposed five-level boost multilevel inverter

The five-boost multilayer inverter is illustrated in Figure 2. The five-level multilevel inverter structure doubles the input voltage and increases the output voltage. Reverse-direction diodes are absent from two of the eight switches in the intended topology. Table 1 illustrates that the five-level output voltage is generated by only six of the twenty-eight toggling states in the proposed inverter. All system functions are represented by the graphics. This is the significance of the numbers three and four. Figure 3a illustrates the system's numerous modes. In Mode 1, the direct current source charges Capacitor C; however, the inverter does not generate any power.

This is referred to as "freewheeling." In this investigation, a capacitor is charged by a substantial inrush current, resulting in a voltage drop to zero. The issue will be present in the preponderance of multilevel topologies that are based on FC. Pre-charged devices may be implemented in high-power applications. These devices gradually elevate the voltage of the capacitor. Only S1, S2, S3, and S4 remain illuminated; all other devices have been deactivated. When the DC source voltage is applied to capacitor C, it undergoes a charge.

When the voltage of capacitor C reaches its steady-state value, it begins to charge. The output terminals, A and B, are connected. In Mode 2, S1, S2, S3, and S5 are operational, while the remaining systems are inactive. The inverter's input and output voltages are identical, as illustrated in Figure 3b. Capacitor C maintains a consistent DC source voltage when it is deactivated. Connect the positive terminals of the input (b) and output (a). Connect Terminal a to the negative terminal of the DC source. In mode 3, switches S3, S5, and S8 are activated, while the remaining switches are deactivated.

The input voltage is doubled by the inverter, as illustrated in Figure 3c. In this case, the negative terminal of capacitor C is connected to output terminal an, while the positive terminal of the DC source is connected to output terminal b. S1, S2, S3, and S4 remain illuminated when all other switches are deactivated. The inverter generates zero output voltage (Fig. 4a) in mode 4, or "freewheeling," while the DC source charges capacitor C.

The voltage of C is equivalent to that of the DC source. In constant state, the applied voltage and charge of capacitor C are equivalent. Switches S1, S2, S4, and S6 are operational in mode 5, while the others are deactivated. Connect the output terminals a and b. The inverter's output voltage is equivalent to the input voltage, as illustrated in Figure 4b. It is powered by the DC supply because its voltage is equivalent to that of C. The positive (a) and negative (b) output terminals are connected to the positive and negative terminals of the DC source, respectively. S4, S6, and S7 employ Mode 6, while the remaining systems do not.

The input voltage is doubled by the inverter's output voltage, as illustrated in Figure 4c. Terminals a and b are used to connect the positive and negative terminals of capacitor C to the direct current source.

2.2 Parameter Design A suitable capacitance is essential for the reduction of voltage ripple. High voltage ripple may

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induce unreliable output voltage increases. This assertion is corroborated by empirical evidence. DC powers 3a, b, 4a, and C. This leads to the formation of these prevalent equations.

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} \quad (1)$$

This is demonstrated. The final decision is still in the hands of C and 4a. This equation differs from the previous one. The statement is expressed as

$$\{v_c = v_{dc} \Leftrightarrow i_c = i_{in} - i_{load} \quad (2)$$

The discharge varieties of C are denoted by numerical values. This equation delineates the characteristics of capacitors in modes 3c and 4b:

$$\{v_c = v_o - v_{dc} \Leftrightarrow i_c = i_{in} \quad (3)$$

The voltage of the capacitor is indicated on the graph. 5. The graph and images 1-3 can be employed to calculate C:

Table 1 Switching states of the five-level inverter

Vector	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	Output
V_0	1	1	1	1	0	0	0	0	0
V_1	1	1	1	0	1	0	0	0	V_{dc}
V_2	0	0	1	0	1	0	0	1	$2V_{dc}$
V_3	1	1	1	1	0	0	0	0	0
V_4	1	1	0	1	0	1	0	0	$-V_{dc}$
V_5	0	0	0	1	0	1	1	0	$-2V_{dc}$

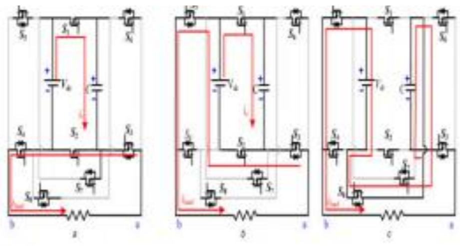

Fig. 3 *Operation modes*
(a) Mode I, (b) Mode II, (c) Mode III

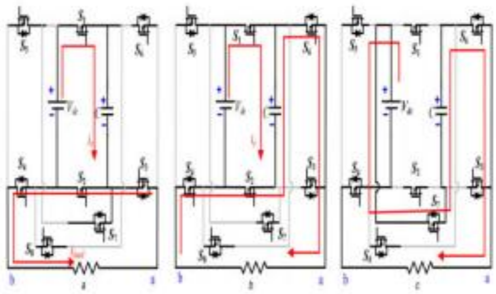

Fig. 4 *Operation modes*
(a) Mode IV, (b) Mode V, (c) Mode VI

$$C = \left(\frac{v_o - v_{dc}}{2\Delta v_c}\right) DT_s \quad (4)$$

The duty ratio D, input voltage vdc, output voltage vo, sampling rate Ts, and capacitor voltage ripple all influence C. Table 2 illustrates the stress components for voltage and current. The pressure in each toggling device is consistent. Numerous voltage deviations have been documented. Voltage stress is elevated in S7 and S8. This is the equivalent of output voltage. The input voltage of the other switches is identical. S7 and S8 are subjected to a greater amount of voltage stress than the other switches as a result of the circuit imbalance. It is imperative to conduct a meticulous assessment of the cultivation of the appropriate constituents.

Level shift pulse width modulation

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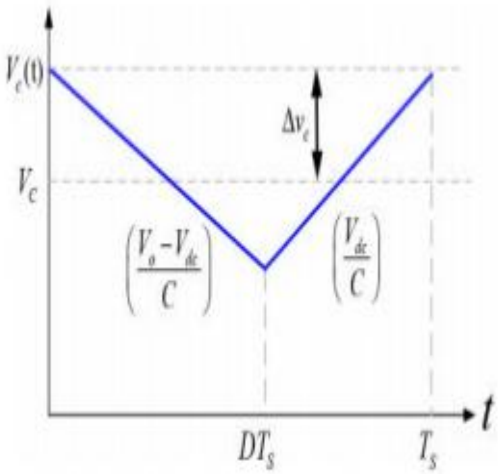

PWM typically employs a predetermined frequency to activate and deactivate DC or AC power converter switches. A waveform with a high modulation index and a lower harmonic profile is generated when the pulse pattern is inputted into the PWM block. Modulation techniques encompass a variety of components, including the mitigation of switching loss. They mitigate current surges and maintain capacitor voltage. The two-level converter transitions can be observed by contrasting the modulation signal with a triangular carrier.

Table 2 Devices voltage and current stress

Device	Voltage stress	Current stress
S_1	V_{in}	I_{in}
S_2	V_{in}	I_{in}
S_3	V_{in}	I_{in}
S_4	V_{in}	I_{in}
S_5	V_{in}	I_{in}
S_6	V_{in}	I_{in}
S_7	V_o	I_{in}
S_8	V_o	I_{in}

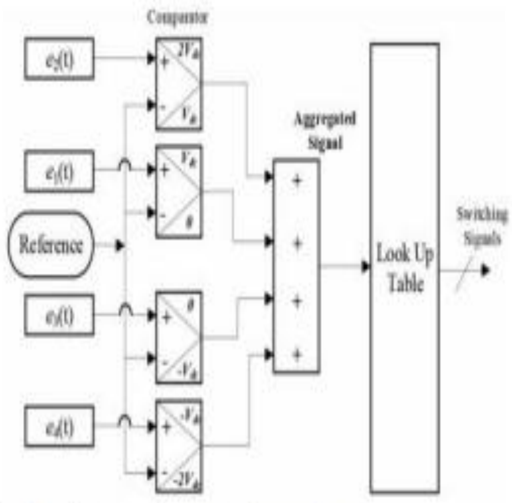

Fig. 6 *Switching signal generation schematic diagram*

5.SIMULATION RESULTS

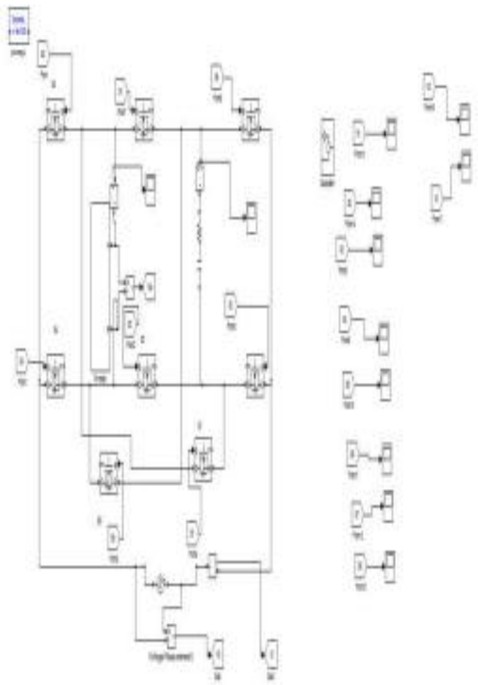

Fig .simulink model

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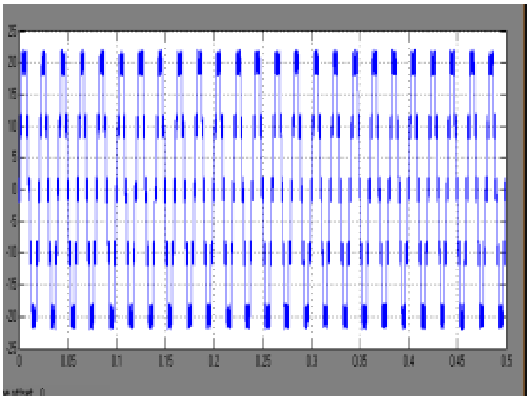

Fig grid currents

Switches cease to conduct electricity when they are activated. Conductive switching devices result in energy loss. Three shifts are necessary for the system to complete all eight switching procedures. This leads to switching and conduction losses. The subsequent sections provide analytical calculations for switching loss and conduction. 4.1 Conduction Losses: The architecture that is recommended contains eight switches, two of which are one-way power switches. The remaining six relays allow for one-way current.

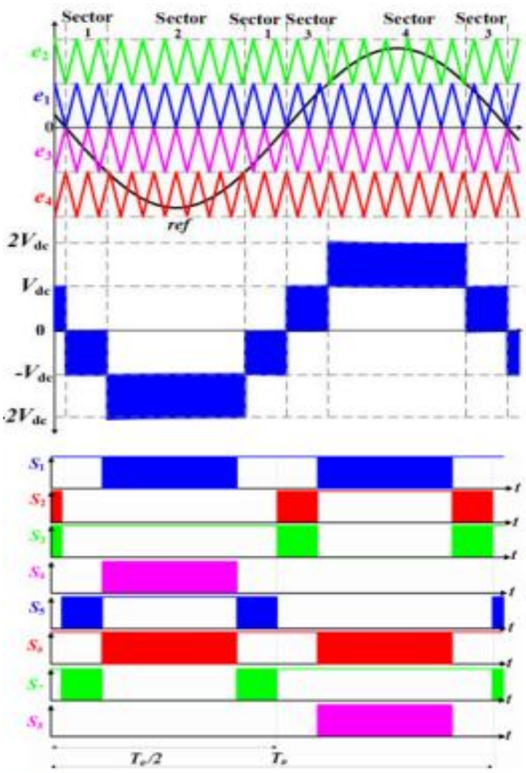

Fig. 8 *Driving signals of the five-level inverter*

Section 2 addresses the instantaneous conduction losses of power switches and body diodes during bidirectional conduction.

$$\rho_{c,T}(t) = [V_T + R_T i^{\alpha}(t)]i(t) \quad (5)$$

$$\rho_{c,D}(t) = [V_D + R_D i(t)]i(t) \quad (6)$$

The average conduction losses are expressed as

$$\rho_{c,avg} = \frac{1}{\Pi}\int_0^{\Pi}\left[\begin{array}{c}\{N_T(t)V_T + N_D(t)V_D\}i_L(t)\\ +\{N_T(t)R_T i_L^{\alpha+1}(t)\} + \{N_D(t) i_L^2(t)\}\end{array}\right]d(\omega t) \quad (7)$$

The variables ρc, avg(t), VT, VD, RT, RD, α, ND, NT, and ρc, T(t), ρc, D(t), VT, VD, RT, RD, α, ND, NT, represent the transistor's on-state voltage drop, the diode's equivalent on-state resistance, constant, the number of conducting diodes, and the semiconductor's instantaneous conduction.

Switching losses

The voltage and current during the transition interval can be linearly estimated to determine the power loss of each device. This method can be employed to determine the amount of electricity consumed during activation.

$$E_{on,j} = \int_0^{t_{on}}\left\{\left[V_{o,j}\frac{t}{t_{on}}\right]\left[-\frac{I}{t_{on}}(t - t_{on})\right]\right\}dt = \frac{1}{6}V_{o,j}It_{on} \quad (8)$$

Similarly, energy losses of the *j*th switch during turning off are calculated as

$$E_{off,j} = \int_0^{t_{off}}\left\{\left[V_{o,j} * \frac{t}{t_{off}}\right]\left[-\frac{I}{t_{off}}(t - t_{off})\right]\right\}dt = \frac{1}{6}V_{o,j}It_{off} \quad (9)$$

The duration, voltage, current, and activation and deactivation periods of the jth switch are represented by symbols. Ton, I, Vo, j, Eoff, j, and Toff are all examples. The total switching power losses are determined using the following formula:

$$\rho_S = \sum_{j=1}^{2n+2}\left[\frac{1}{6}V_{o,j} * I(t_{on} + t_{off})f_j\right]$$

Fig. displays a graph of inverter efficiency. 9. The recommended inverter works best

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with 350 to 650 watts of power. Up to 800 W, it is more than 95% efficient across the entire power range.

6..CONCLUSION

A multilevel inverter with five stages of boost was examined in this investigation. The single-phase version necessitates eight valves and a DC capacitor. The output may contain five levels if the amplitude exceeds twice the input voltage. The equilibrium issue is resolved by this arrangement, which utilizes only one capacitor. The recommended inverter is optimal for solar power systems due to its capacity to augment electricity generation. After charging, the DC capacitor is connected in series with the DC source. The voltages that are released increase. LS-PWM is employed to regulate the switches of inverters. The capacitor can be charged by state changes without affecting the voltage.

Table 3 Component requirements for single-phase five-level multilevel inverter

Topology	NPC [34]	FC [19]	CHB [35]	[10]	[36]	Diode clamped [37]	Capacitor clamped [38]	This work
number of main switches	8	8	8	4	5	8	12	8
number of diodes	0	0	0	4	4	6	0	2
number capacitors	3	3	0	2	2	4	4	1
number of dc-source	1	1	2	1	1	1	1	1

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